REMARKS

Claims 4-9, 11, 13, and 14, are pending in the application. Claims 1-3, 10, and 12, have been withdrawn from further consideration as being directed to a non-elected invention. Claim 14 has been added. Reconsideration and allowance of all claims are respectfully requested in view of the following remarks.

The Applicants respectfully request that the Examiner acknowledge receipt of one (1) sheet of Proposed Drawing Corrections which amends Fig. 6 to add reference numeral --1-- for reasons of clarity, and reference numeral --201-- which is discussed in the specification at page 5, paragraph 1, but not shown in the drawings.

The Examiner has objected to Claims 11 and 13 for improper multiple dependency. The claims have been amended to obviate any improper multiple dependency noted by the Examiner.

The Examiner has rejected Claims 4-6 under 35 U.S.C. §102(e) as being anticipated by Kawasaki et al. The Examiner has rejected Claims 7 and 8 under 35 U.S.C. §103 as being unpatentable over Kawasaki et al. However, the Examiner has found Claim 9 allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims. Claim 9 has been rewritten into independent form as new Claim 14, and Claim 14 should now be allowed. For the following reasons, the prior art rejections are respectfully traversed.

The present invention relates to a method of making a bottom-gate thin-film transistor comprising forming a gate electrode on a substrate; forming a gate insulating film on the gate electrode; forming a laminate comprising a precursor film for an active layer, and a protective insulating film on the gate insulating film, the protective insulating film having a thickness of 100 nm or less; implanting a dopant in one of an LDD region and a source-drain region of the precursor film for the active layer through the protective insulating film without etching; and activating the implanted dopant so that a non-doped portion comprises the active layer.

Kawasaki et al. disclose manufacturing simultaneously TFT's for a pixel portion and for a driver circuit provided in the periphery of the pixel portion.

The Applicants respectfully submit that Kawasaki et al. do not teach or suggest a method of making a bottom-gate thin-film transistor including the step of implanting a dopant in one of an LDD region and a source-drain region of the precursor film for the active layer through the protective insulating film without etching; as recited in amended Claim 4.

Rather, contrary to the claims of the present invention, Kawasaki et al. teach performing an etching treatment on the first spacer film and the second spacer film 110 (which the Examiner equates to the protective insulating film 8 of the present invention) to expose the crystalline silicon film 106 (which the Examiner equates to the precursor film for the active layer 7 of the present invention) and doping with an impurity element for imparting P type to form a source region and a drain region in the P channel type TFT of the driver circuit (see Kawasaki et al., col. 7, lines 9-32).

However, in the present invention, when forming an LDD region or a source-drain region, a dopant is injected through the insulating film 8, without etching the protective insulating film 8; thereby, the etching process of the protective insulating film 8 in the conventional method can be eliminated, thus improving productivity (see page 12 of the present specification, at lines 13-22).

Accordingly, Claim 4 is not anticipated by (nor obvious over) Kawasaki et al., and the rejection of Claim 4 under 35 U.S.C. §102(e) should be withdrawn.

Further, since Claims 5-9, 11 and 13, depend from Claim 4, they are also patentably distinguishable over Kawasaki et al. for the reasons cited above with respect to Claim 4.

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 19-3140.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 6, the second full paragraph, continuing to page 7, was amended as follows:

[The present inventors have found that, by] By setting the thickness of the protective insulating film 8 at 100 nm or less instead of approximately 200 nm in the process for fabricating the conventional bottom-gate TFT, and by injecting the dopant through the protective insulating film 8 when the LDD region 9, or the source-drain region 10 is formed subsequently, it is possible to eliminate the etching step of the protective insulating film 9 and also an insufficient breakdown voltage of the gate insulating film 6 can be overcome. Moreover, it has also been found that the structure of such a TFT or the method for fabricating the same can be employed for liquid crystal display devices and organic EL devices driven by TFTs.

IN THE CLAIMS:

The claims were amended as follows:

4. (Amended) A method [for] of making a bottom-gate thin-film transistor comprising:

[a step (1) of] forming a gate electrode on a substrate;

[a step (2) of] forming a gate insulating film on the gate electrode;

[a step (3) of] forming a laminate comprising a precursor film for an active layer, and a protective insulating film on the gate insulating film, the protective insulating film having a thickness of 100 nm or less;

[a step (4) of] implanting a dopant in one of an LDD region [or] and a source-drain region of the precursor film for the active layer through the protective insulating film without etching; and

[a step (5) of] activating the implanted dopant so that a non-doped portion [constitutes] comprises the active layer.

5. (Amended) [A] The method of [for] making a bottom-gate thin-film transistor according to Claim 4, wherein the active layer comprises a polysilicon film.

6. (Amended) [A] The method of [for] making a bottom-gate thin-film transistor according to Claim 5, wherein, in the [step (3)] laminate forming step, an amorphous silicon film is formed on the gate insulating film, the amorphous silicon film is crystallized to form the polysilicon film, and the protective insulating film is formed on the polysilicon film.

7. (Amended) [A] The method [for] of making a bottom-gate thin-film transistor according to Claim 5, wherein, in the [step (3)] laminate forming step, an amorphous silicon film is formed on the gate insulating film, the protective insulating film is continuously formed on the amorphous silicon film, and then the amorphous silicon film is crystallized to form the polysilicon film.

8. (Amended) [A] The method [for] of making a bottom-gate thin-film transistor according to Claim 5, wherein, in the [step (3)] laminate forming step, an amorphous silicon film is formed on the gate insulating film, the protective insulating film is formed on [the] a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is crystallized to form the polysilicon film.

9. (Amended) A method [for] of making a bottom-gate thin-film transistor according to [any one of Claims] Claim 4 [to 8], wherein, subsequent to the [step (4)] dopant implanting step, defects formed in the protective insulating film are recovered.

11. (Amended) A method [for] of fabricating a liquid crystal display device comprising [the steps of]:

making a bottom-gate thin-film transistor by a method according to any one of Claims 4 to 9;

forming an interlayer insulating film, a transparent electrode, and an alignment layer on a protective insulating film of the bottom-gate thin-film transistor to [constitute] comprise a TFT substrate; and

interposing a liquid crystal between the TFT substrate and a counter substrate provided with a counter electrode.

13. (Amended) A method [for] of fabricating an organic EL device comprising [the steps of]:

making a bottom-gate thin-film transistor by a method according to any one of Claims 4 to 9;

forming an interlayer insulating film on a protective insulating film of the bottom-gate thin-film transistor; and

forming an organic EL element driven by the bottom-gate thin-film transistor on the interlayer insulating film.

Claim 14 was added.